02-02-00 A

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.: 2933SE-88

Inventors: Tomomichi NAKAI of 2-18, Sanbongi, Ogaki-shi, Gifu-ken 503-0813 Japan
Toshio NAKAKUKI of 1069-5, Honden, Hozumi-cho, Motosu-gun, Gifu-ken 501-0236 Japan

Express Mail Label No.: **IB914059135**

Title: "CLOCK SIGNAL GENERATOR FOR SOLID-STATE IMAGING APPARATUS"

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

Enclosed for filing with the above-identified utility patent application, please find the following:

1. [X] Specification (Total Pages of Text, including Abstract and Claims: 12)
2. [X] Drawing(s) (35 USC 113) (Total Sheets: 2) [X] FORMAL [] INFORMAL
3. [X] Oath or Declaration (Total Pages: 3) [X] Signed [] Unsigned
4. [X] Assignment Papers *(cover sheet & document(s))*
5. [X] Return Postcard (MPEP 503) *(should be specifically itemized)*
6. [X] A check in the amount of $690.00 is enclosed.

FEE CALCULATION:

	(COL. 1) NO. FILED			(COL. 2*) NO. EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE		LARGE ENTITY RATE	LARGE ENTITY FEE
BASIC FEE:						$345.00	OR		$690.00
TOTAL CLAIMS:	5	-	20	0	X $9 =		OR	X $18 =	$0.00
INDEP. CLAIMS:	2	-	3	0	X $39 =		OR	X $78 =	$0.00
MULTIPLE DEPENDENT CLAIMS					+ $130 =		OR	+$260 =	$0.00
*IF THE DIFFERENCE IN COL. 2 IS LESS THAN ZERO, ENTER "O" IN COL. 2.					TOTAL:				$690.00

OTHER INFORMATION:

1. [X] The Commissioner is hereby authorized to debit any underpayments or credit any overpayment to Deposit Account No. 19-1970.

2. [X] The Commissioner is hereby authorized to charge all required fees for extensions of time under §1.17 to Deposit Account No. 19-1970.

3. [X] Foreign Priority benefits are claimed under 35 USC §119 of Japanese Patent Application Serial No. 11-023883 filed February 1, 1999.

4. Correspondence Address:

Douglas W. Swartz
SHERIDAN ROSS P.C.
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
Telephone: (303) 863-9700
Facsimile: (303) 863-0223

Respectfully Submitted,

SHERIDAN ROSS P.C.

Douglas W. Swartz

Date: Jan. 31, 2000

Douglas W. Swartz
Registration No. 37,739

CLOCK SIGNAL GENERATOR FOR SOLID-STATE IMAGING APPARATUS

BACKGROUND OF THE INVENTION

The present invention relates to a solid-state imaging apparatus having a frame transfer or frame interline type solid-state imaging device.

Fig. 1 is a block diagram showing an imaging apparatus that has a frame transfer type CCD 1 (solid-state imaging device). Fig. 2 is a timing chart illustrating the operation of the imaging apparatus.

The CCD 1 includes a light receiving portion 1a, a storing portion 1b, a horizontal transfer portion 1c, and an output portion 1d. The light receiving portion 1a has a plurality of shift registers arranged parallel to one another in the vertical direction. Each bit of the shift registers forms a light receiving pixel. Each light receiving pixel stores an information charge generated in correspondence with a sensed object. The storing portion 1b has a plurality of shift registers arranged continuously from the shift registers of the light receiving portion 1a. Further, the storing portion 1b temporarily stores information charges that correspond to a single image output by the light receiving portion 1a. The number of bits in each shift register is determined in accordance with the number of bits in the shift registers of the light receiving portion 1a. The horizontal transfer portion 1c has a single shift register, each bit of which is connected to the output of an associated storing portion 1b shift register. Further, the horizontal transfer portion 1c receives the information charges, which correspond to a single image,

line by line and sequentially transfers each line of information charges. The output portion 1d has an electrically independent capacitor and an amplifier for extracting fluctuations in the potential of the capacitor. The capacitor receives the information charge from the horizontal transfer portion 1c in units of single pixels. The output portion 1d converts the information charge into a voltage value and generates an image signal Y.

A vertical drive circuit 2, which is operated in accordance with a vertical timing signal VD, generates a vertical transfer clock ϕv from a reference clock MCK, which has a predetermined cycle, and sends the vertical transfer clock ϕv to the light receiving portion 1a and the storing portion 1b. When the light receiving portion 1a receives the vertical transfer clock ϕv, the information charges stored in the light receiving pixels are immediately transferred to the storing portion 1b in units of single images. A horizontal drive circuit 3, which is operated in accordance with a horizontal timing signal HD, generates a storage transfer clock ϕs from the reference clock MCK. The horizontal drive circuit 3 simultaneously generates a horizontal transfer clock ϕh. The storage transfer clock ϕs is provided to the storing portion 1b together with the vertical transfer clock ϕv. When the storing portion 1b receives the storage transfer clock ϕs, the information charges stored in the storing portion 1b are transferred to the horizontal transfer portion 1c line by line. The horizontal transfer clock ϕh is provided to the horizontal transfer portion 1c. When the horizontal transfer portion 1c receives the horizontal transfer clock ϕh, the information charges transferred to the horizontal transfer portion 1c from the storing portion 1b are sequentially,

serially transferred to the output portion 1d.

A timing control circuit 4 includes a horizontal counter and a vertical counter. The horizontal counter divides the reference clock MCK to generate the horizontal timing signal HD. The vertical counter divides this horizontal timing signal HD to generate the vertical timing signal VD. For example, in accordance with the NTSC standards, the timing control circuit 4 divides the reference clock MCK, the frequency of which is 14.32MHz, by 910 to generate the horizontal timing signal HD and this horizontal timing signal HD by 252.5 to generate the vertical timing signal VD. The horizontal and vertical timing signals HD, VD respectively represent various timing signals related with horizontal scan periods and vertical scan periods.

The CCD 1 repeats imaging operations in cycles corresponding to the vertical timing signal VD and outputs the image signal Y in units of single lines in cycles corresponding to the horizontal timing signal HD during each vertical scan period.

The exposure time of the CCD 1, or the time period during which an information charge is stored in each light receiving pixel, coincides with the vertical scan cycle when an electronic shutter is not operated. Further, the exposure time may normally be varied by discharging the information charges during the vertical scan period, that is, by operating an electronic shutter. If the imaging apparatus does not have television system restrictions, the frequency of the reference clock MCK may be changed to vary the exposure time.

If the sensed object has a low luminance or if the CCD 1 has a low light receiving sensitivity, the frequency of the reference clock MCK is decreased to lengthen the vertical scan cycle in order to obtain sufficient exposure time. However, when the frequency of the reference clock MCK is decreased, the frequency of the vertical transfer clock ϕv, which is generated from the reference clock MCK, also decreases. This increases the time required for frame transfer from the light receiving portion 1a to the storing portion 1b and increases smear.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a solid-state imaging apparatus that minimizes the mixing of smear components during frame transfer even when the exposure time of the imaging device is increased.

To achieve the above object, the present invention provides a solid-state imaging apparatus comprising a solid-state imaging device including a light receiving portion having a plurality of light receiving pixels, a storing portion arranged adjacent to the light receiving portion, and a horizontal transfer portion arranged adjacent to the storing portion. A timing control circuit divides a first clock having a predetermined cycle to generate a vertical scan timing signal and a horizontal scan timing signal. A vertical drive circuit is connected to the timing control circuit for generating a vertical transfer clock from a second clock, the cycle of which is shorter than the first clock, in accordance with the vertical scan timing signal. The vertical transfer clock is used to transfer information charges accumulated in the light receiving pixels of the light receiving portion to the storing portion. A

horizontal drive circuit is connected to the timing control circuit for generating a horizontal transfer clock from the first clock in accordance with the horizontal scan timing signal. The horizontal transfer clock is used to output the information charges transferred from the storing portion to the horizontal transfer portion.

A further aspect of the present invention provides a method for driving a solid-state imaging device including a light receiving portion having a plurality of light receiving pixels, a storing portion arranged adjacent to the light receiving portion, and a horizontal transfer portion arranged adjacent to the storing portion. The method includes the steps of dividing a reference clock with a predetermined dividing ratio to generate a divisional clock having a cycle longer than the cycle of the reference clock, generating a vertical scan timing signal and a horizontal scan timing signal from the divisional clock, generating a vertical transfer clock from the reference clock in accordance with the vertical scan timing signal, providing the vertical transfer clock to the light receiving portion and the storing portion in order to transfer information charges accumulated in the light receiving pixels of the light receiving portion to the storing portion, generating a horizontal transfer clock from the divisional clock in accordance with the horizontal scan timing signal, and providing the horizontal transfer clock to the horizontal transfer portion in order to output the information charges transferred from the storing portion to the horizontal transfer portion.

Other aspects and advantages of the present invention will become apparent from the following description, taken in conjunction with the accompanying drawings, illustrating

by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention, together with objects and advantages thereof, may best be understood by reference to the following description of the presently preferred embodiments together with the accompanying drawings in which:

Fig. 1 is a schematic block diagram showing a prior art solid-state imaging apparatus;

Fig. 2 is a timing chart showing the operation of the solid-state imaging apparatus of Fig. 1;

Fig. 3 is a schematic block diagram showing a solid-state imaging apparatus according to the present invention; and

Fig. 4 is a timing chart showing the operation of the solid-state imaging apparatus of Fig. 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A solid-state imaging apparatus according to the present invention will now be described with reference to Figs. 3 and 4.

Referring to Fig. 3, a CCD 11 (solid-state imaging device) includes a light receiving portion 11a, a storing portion 11b, a horizontal transfer portion 11c, and an output portion 11d. The information charges stored in the light receiving portion 11a are transferred to the output portion 11d via the storing portion 11b and the horizontal transfer portion 11c. The output portion 11d generates an image signal Y based on the information charges.

A vertical drive circuit 12, which is operated in

accordance with a vertical timing signal VD, generates a vertical transfer clock ϕv from a reference clock MCK, which has a predetermined cycle, and sends the vertical transfer clock ϕv to the light receiving portion 11a and the storing portion 11b. When the light receiving portion 11a receives the vertical transfer clock ϕv, the information charges stored in light receiving pixels are immediately transferred to the storing portion 11b in units of single images.

A horizontal drive circuit 13, which is operated in accordance with a horizontal timing signal HD, generates a storage transfer clock ϕs from a divisional clock DCK, which is generated by a frequency dividing circuit 15. The horizontal drive circuit 13 simultaneously generates a horizontal transfer clock ϕh. The storage transfer clock ϕs is provided to the storing portion 11b. The information charges stored in the storing portion 11b are transferred to the horizontal transfer portion 11c line by line in accordance with the storage transfer clock ϕs. The information charges transferred to the horizontal transfer portion 11c from the storing portion 11b are sequentially, serially transferred to the output portion 11d in accordance with the horizontal transfer clock ϕh.

A timing control circuit 14 includes a horizontal counter and a vertical counter. The horizontal counter divides the divisional clock DCK to generate the horizontal timing signal HD. The vertical counter divides the horizontal timing signal HD to generate the vertical timing signal VD. The vertical and horizontal timing signals VD, HD are provided to the vertical and horizontal drive circuits 12,13, respectively.

The dividing circuit 15 divides the reference clock

signal MCK with a predetermined dividing ratio to generate the divisional clock DCK. For example, if the dividing circuit 15 divides the frequency of the reference clock MCK into two, the cycles of the vertical timing signal VD and the horizontal timing signal HD generated by the timing control circuit 14 become two times longer. In this case, the frame transfer cycle in the CCD 11 becomes two times longer, and the storing period of the information charges increases by two times. In this state, the vertical drive circuit 12 generates the vertical transfer clock ϕv by synthesizing the reference clock MCK that does not pass through the dividing circuit 15. Accordingly, the time required for frame transfer remains short even if the cycle of the vertical timing signal VD becomes long. This prevents smear components from increasing.

In addition to setting the information charge storing time of the CCD 11 in accordance with the cycle of the vertical timing signal VD, the information charge storing time may be set by operating an electronic shutter to temporarily discharge the information charge during the vertical scan period. The dividing ratio of the dividing circuit 15 may be variable so that an appropriate value can be selected to change the information charge storing time of the CCD 11. The variable dividing ratio of the dividing circuit 15 may be used in combination with an electronic shutter to adjust the information charge storing time when necessary.

In the preferred embodiment, the dividing circuit 15 provides the dividing clock DCK to the timing control circuit 14 in order to lengthen the vertical scan period. In this state, the cycle of the reference clock MCK received by the vertical drive circuit 12 is shorter than the cycle

of the divisional clock DCK. Thus, the frequency of the vertical transfer clock ϕv is not decreased, and a smear increase that would be caused by a longer frame transfer time is prevented.

Instead of the frame transfer type CCD 11, the present invention may be applied to a frame interline transfer type CCD in which a vertical transfer portion is arranged between each row of light receiving pixels in the storing portion.

It should be apparent to those skilled in the art that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. Therefore, the present examples and embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalence of the appended claims.

WHAT IS CLAIMED IS:

1. A solid-state imaging apparatus comprising:

a solid-state imaging device including a light receiving portion having a plurality of light receiving pixels, a storing portion arranged adjacent to the light receiving portion, and a horizontal transfer portion arranged adjacent to the storing portion;

a timing control circuit for dividing a first clock having a predetermined cycle to generate a vertical scan timing signal and a horizontal scan timing signal;

a vertical drive circuit connected to the timing control circuit for generating a vertical transfer clock from a second clock, the cycle of which is shorter than the first clock, in accordance with the vertical scan timing signal, wherein the vertical transfer clock is used to transfer information charges accumulated in the light receiving pixels of the light receiving portion to the storing portion; and

a horizontal drive circuit connected to the timing control circuit for generating a horizontal transfer clock from the first clock in accordance with the horizontal scan timing signal, wherein the horizontal transfer clock is used to output the information charges transferred from the storing portion to the horizontal transfer portion.

2. The solid-state imaging apparatus according to claim 1, further comprising a dividing circuit connected to the timing control circuit for generating the first clock by dividing the second clock.

3. The solid-state imaging apparatus according to claim 2, wherein a dividing ratio of the second clock in the dividing circuit is variably set in accordance with the information

charge storing time of the solid-state imaging device.

4. A method for driving a solid-state imaging device including a light receiving portion having a plurality of light receiving pixels, a storing portion arranged adjacent to the light receiving portion, and a horizontal transfer portion arranged adjacent to the storing portion, the method comprising the steps of:

dividing a reference clock with a predetermined dividing ratio to generate a divisional clock having a cycle longer than the cycle of the reference clock;

generating a vertical scan timing signal and a horizontal scan timing signal from the divisional clock;

generating a vertical transfer clock from the reference clock in accordance with the vertical scan timing signal;

providing the vertical transfer clock to the light receiving portion and the storing portion in order to transfer information charges accumulated in the light receiving pixels of the light receiving portion to the storing portion;

generating a horizontal transfer clock from the divisional clock in accordance with the horizontal scan timing signal; and

providing the horizontal transfer clock to the horizontal transfer portion in order to output the information charges transferred from the storing portion to the horizontal transfer portion.

5. The driving method according to claim 4, further comprising a step of varying the predetermined dividing ratio in accordance with the information charge storing time of the solid-state imaging device.

ABSTRACT OF THE DISCLOSURE

A frame transfer type solid-state imaging apparatus has a matrix of pixels which store information charges corresponding to a received image. The information charges are moved from the pixels to vertical transfer registers, and then to a horizontal transfer register, prior to being stored. A timing control circuit generates a vertical scan timing signal and a horizontal scan timing signal using a divided clock signal. A horizontal drive circuit generates a horizontal transfer clock using the divided clock signal and the horizontal scan timing signal. The horizontal transfer clock is used to move the information charges from the vertical transfer registers to the horizontal transfer register. A vertical drive circuit generates a vertical transfer clock using a reference clock signal and the vertical scan timing signal. The vertical transfer clock is used to move the information charges from the pixels to the vertical transfer registers. The divided clock signal is generated by dividing the reference clock signal by a predetermined ratio, such that the divided clock signal is longer than the reference clock signal. By generating the vertical transfer clock using the reference clock, and not the longer, divided clock, the resulting image does not have an increase in smear components.

Fig.1 (Prior Art)

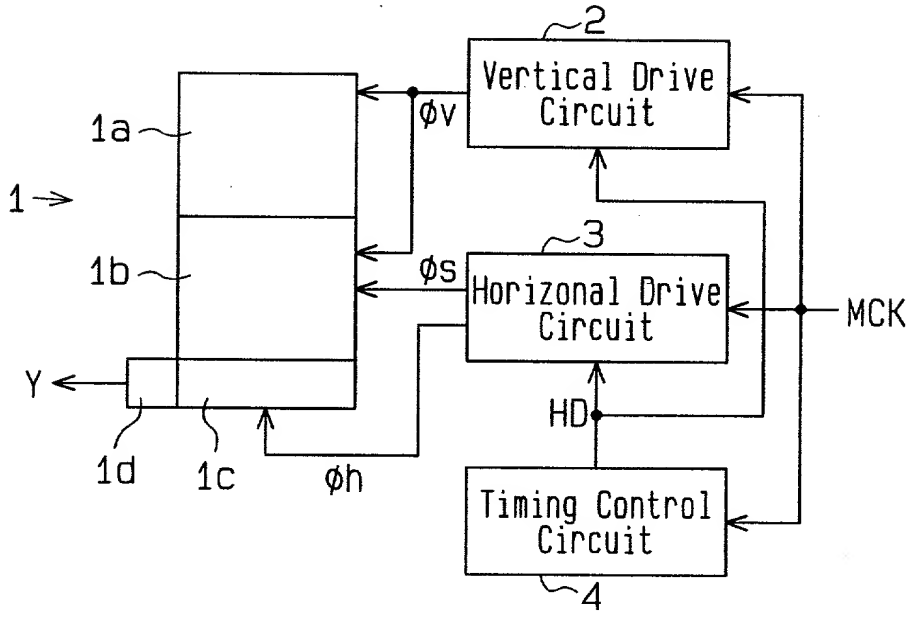


Fig.2 (Prior Art)

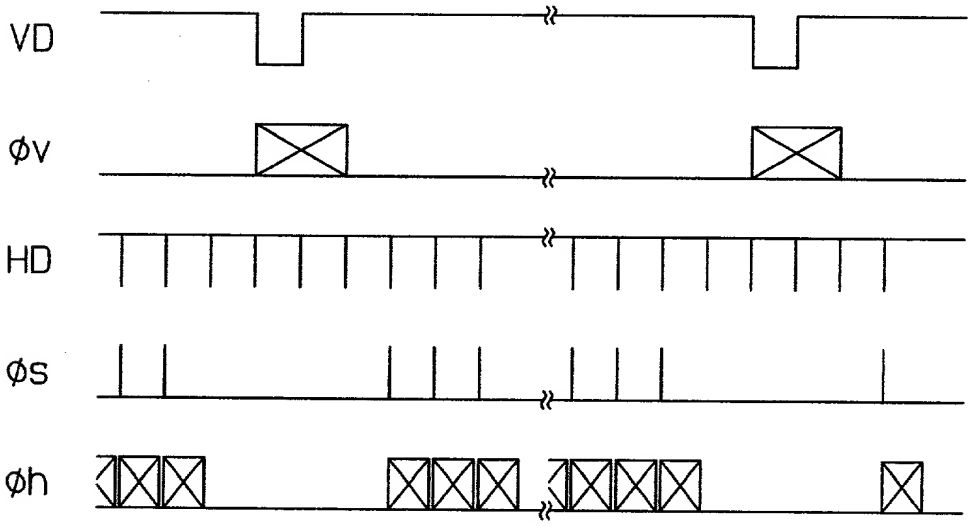


Fig.3

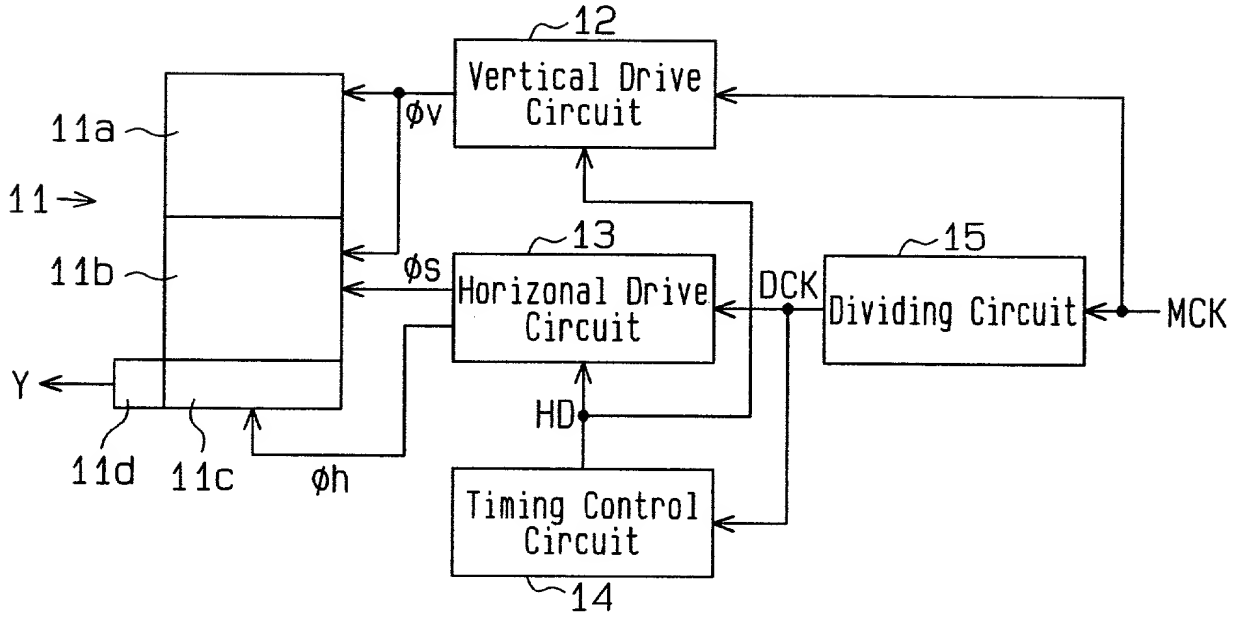
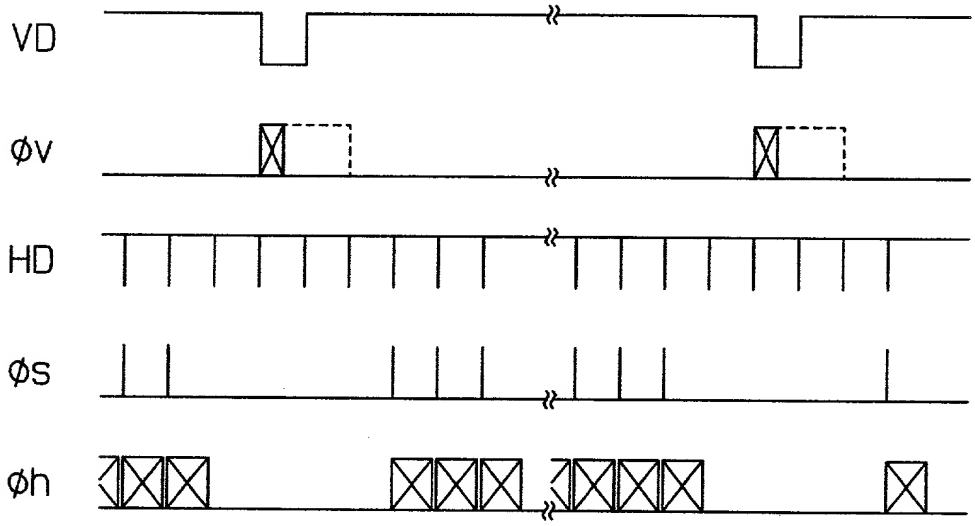

12
Vertical Drive Circuit
φv
11a
11
11b
13
φs
Horizonal Drive Circuit
DCK
15
Dividing Circuit
MCK
Y
HD
11d
11c
φh
Timing Control Circuit
14

Fig.4


VD
φv
HD
φs
φh

Declaration and Power of Attorney For Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

_____

_____

_____

その明細書を
（該当する方に印を付す）

☐ ここに添付する。

☐ _____ 日に出願番号

第 _____ 号として提出し、

_____ 日に補正した。
（該当する場合）

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

私は、連邦規則法典第37部第１章第56条（ａ）項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CLOCK SIGNAL GENERATOR FOR SOLID-STATE IMAGING APPARATUS

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as

Application Serial No. _____

and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Form PTO-FB-265 (8-83)

Patent and Trademark Office-U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration

私は、合衆国法典第35部第119 条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

(Number) (番 号)	(Country) (国 名)	(Day/Month/Year Filed) (出願の年月日)	Priority claimed 優先権の主張	
Pat. Appln. No. 11-023883	Japan	01 / 02 / 1999	[X] Yes あり	[ ] No なし
			[ ] Yes あり	[ ] No なし
			[ ] Yes あり	[ ] No なし

私は、合衆国法典第35部第120 条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112 条第１項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはＰＣＴ国際出願日の間に公表された連邦規則法典第37部第１章第56条（ａ）項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現 況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損うことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

委任状：私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する。
（代理人氏名および登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*list name and registration number*)

David F. Zinger, Registration No. 29,127; Craig C. Groseth, Registration No. 31,713; Michael L. Tompkins, Registration No. 30,980; Todd P. Blakely, Registration No. 31,328; Gary J. Connell, Registration No. 32,020; Wannell M. Crook, Registration No. 31,071; Sabrina Crowley Stavish, Registration No. 33,374; Lewis D. Hansen, Registration No. 35,536; Joseph E. Kovarik, Registration No. 33,005; Douglas W. Swartz, Registration No. 37,739; John C, Scott, Registration No. 38,613; Bruce A. Kugler, Registration No. 38,942; Robert R. Brunelli, Registration No. 39,617; Chester E. Martine, Jr., Registration No. 19,711; Richard L. Hughes, Registration No. 31,264; Tejpal S. Hansra, Registration No. 38,172; Dana L. Hartje, Registration No. 40,638; Don D. Cha, Registration No. 40,945, of SHERIDAN ROSS P.C., 1700 Lincoln Street, Suite 3500, Denver, Colorado 80203.

書類の送付先：

Send Correspondence to:

SHERIDAN ROSS P.C.
1560 Broadway
Suite 1200, Denver
Colorado 80202-5141

直通電話連絡先：（名称および電話番号）

Direct Telephone Calls to: (*name and telephone number*)

(303) 863-9700

唯一のまたは第一の発明者の氏名	Full name of sole or first inventor Tomomichi NAKAI
同発明者の署名　日付	Inventor's signature　Date Tomomichi Nakai　January 25, 2000
住所	Residence Ogaki-shi, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address 2-18, Sanbongi, Ogaki-shi, Gifu-ken 503-0813
	Japan
第2の共同発明者の氏名（該当する場合）	Full name of second joint inventor, if any Toshio NAKAKUKI
同第2発明者の署名　日付	Second Inventor's signature　Date Toshio Nakakuki　January 25, 2000
住所	Residence Gifu-ken, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address 1069-5, Honden, Hozumi-cho, Motosu-gun,
	Gifu-ken 501-0236 Japan

（第六またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for third and subsequent joint inventors.)